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10/571,720	03/13/2006	Tetsuo Nomoto	97929096653	7788

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EXAMINER	
FLOHRE, JASON A	
ART UNIT	**PAPER NUMBER**
4112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/571,720	NOMOTO ET AL.	
	Examiner	Art Unit	
	JASON FLOHRE	4112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/13/206 & 04/02/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element 31 of figure 2 (discussed in paragraph 35, line 3) and element 40 of figure 8 (discussed in paragraph 60, line 4). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show a chip for processing the signal output through the signal line (paragraph 16, lines 1 and 2), VDRV (paragraph 29 line 12), and HDRV (paragraph 36 line 9) as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "38 (figure 2)" and "35 (paragraph 37, line 8)" have both been used to designate the output amplifier. Also, reference characters "32 (figure 2)"

and "35 (paragraph 37, line 9)" have both been used to designate the horizontal signal line. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because in figure 2 element 34 the text reads "SFR"; this should be corrected to read "HSFR" as it is labeled in paragraph 36 line 8. In figure 4 an arrow should be placed pointing from the text “RISING/FALLING TIMES…” to the rise time of the left side of graph (A). In figure 7, the arrow pointing from the text “WHEN TURNING OFF RESET...” to the right side of the first reset pulse should be removed. The potential at that point does not continue from the "GROUND LEVEL” to the “NEGATIVE POTENTIAL”. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be

removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because figures 4b (paragraph 39 lines 2-5), 5b (paragraph 46 lines 10-15), 6b (paragraph 47 lines 17-18), and 7b (paragraph 48 lines 4-6) should all show the voltage level to be at a negative voltage and not at zero volts (in the nonselected state the reset transistor is off). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each

drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: in paragraph 20 line 8 “drain lien” should be "drain line", in paragraph 21 line 4 "for example" should be deleted, in paragraph 22. In the Description of Notations, paragraph 22, elements 100-105, N101, and 40-43 are not listed. In paragraph 31 line 5 “ND11” should be “N11”. In paragraph 39 line 11 “N11” should be “VN11”. In paragraph 44 line 9 “A” should be “a”. In paragraph 44 line 16 “internallt” should be “internally”. In paragraph 50 line 2 “N1” should be “N11”. In line 3 of paragraph 50 “dd” should be “Vdd”. In paragraph 56 line 5 “N1” should be “N11”. In paragraph 60 line 7 “he” should be “the”. In paragraph 63 line 10-11 “imaging image” should be “image”.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (Japanese patent application publication JP-2003-230055), hereinafter referenced as Nakamura.

Regarding claim 1, Nakamuara discloses a solid state imaging device has a plurality of unit pixels formed in an imaging area (figure 9), wherein each unit pixel has a photoelectric converter for generating a charge in accordance with an amount of incident light (1-1 figure 9), a transfer transistor for transferring a signal of the photoelectric converter to a floating node (2-1 figure 9), an amplifier transistor for outputting a signal of the floating node to a signal line (3-1 figure 9), and a reset transistor for resetting the floating node (4-1 figure 9), at least one of a plurality of potentials supplied to a gate electrode of the reset transistor being a negative potential (20-1 figure 12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Hashimoto (United States patent 5,288,988), hereinafter referenced as Hashimoto.

Regarding claim 2, Nakamura discloses a solid state imaging device with a unit pixel (figure 9) having: a photoelectric converter for generating a charge in accordance with an amount of incident light (1-1 figure 9), a transfer transistor for transferring a signal of the photoelectric converter to a floating node (2-1 figure 9), an amplifier transistor for outputting a signal of the floating node to a signal line (3-1 figure 9), and a reset transistor for resetting the floating node (4-1 figure 9), however, Nakamura fails to disclose a portion able to supply three or more types of potentials to the gate electrode of the reset transistor. However, the examiner maintains that it was well known in the art to provide a portion able to supply three or more types of potentials to the gate electrode of the reset transistor, as taught by Hashimoto.

In a similar field of endeavor Hashimoto discloses a photoconversion device having reset control circuitry. In addition, Hashimoto discloses a unit pixel (1 figure 1) which has a reset transistor (M figure 1) who's gate is supplied a voltage waveform (ϕ12 figure 2) and the reset transistor and waveform read on “a portion able to supply three

or more types of potentials to the gate electrode of the reset transistor", as disclosed at column 3, lines 32-33.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura by specifically providing a portion able to supply three or more types of potentials to the gate electrode of the reset transistor, as taught by Hashimoto for the purpose of not subjecting the reset gate supply line to an excessive total voltage swing.

Regarding claim 3, Nakamura and Hashimoto disclose everything claimed as applied above (see claim 2), further the combination discloses wherein the voltage of at least one type of potential among at least three or more types of potentials supplied to the gate electrode of the reset transistor is a negative potential, specifically Hashimoto.

In a similar field of endeavor Hashimoto discloses a photoconversion device having reset control circuitry. Hashimoto discloses a waveform (ϕ12 figure 2) which is supplied to the gate of the reset transistor (M figure 1). Said waveform contains a negative voltage. The waveform and reset transistor read on "wherein the voltage of at least one type of potential among at least three or more types of potentials supplied to the gate electrode of the reset transistor is a negative potential", as disclosed at column 3, lines 32-33.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura by specifically providing wherein the voltage of at least one type of potential among at least three or more types of potentials

supplied to the gate electrode of the reset transistor is a negative potential, as taught by Hashimoto, for the purpose of reducing dark-current and providing a better image.

Regarding claim 4, Nakamura and Hashimoto disclose everything claimed as applied above (see claim 3), further the combination discloses wherein the device has a portion able to set the gate potential when bringing the reset transistor from an ON state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential, specifically, Hashimoto.

In a similar field of endeavor Hashimoto discloses a photoconversion device having reset control circuitry. Hashimoto discloses a waveform (ϕ12 figure 2) which is supplied to the gate of the reset transistor (M figure 1). Said waveform contains a portion which starts at a positive high voltage level, pauses at the GND level, and continues to a negative voltage level. The waveform demonstrates an output from a portion of the device which reads on "wherein the device has a portion able to set the gate potential when bringing the reset transistor from an ON state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential", as disclosed in at column 3, lines 32-33.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura by specifically providing wherein the device has a portion able to set the gate potential when bringing the reset transistor from an ON state to an OFF state at a negative power source potential after passing a

ground level power source potential from a positive high level power source potential, as taught by Hashimoto, for the purpose of not subjecting the signal line to an excessive total voltage swing.

Regarding claim 5, Nakamura and Hashimoto disclose everything claimed as applied above (see claim 3), further the combination discloses wherein at both timings of sampling and holding a precharge phase and a data phase, the gate potential of the reset transistor is set at the ground potential, specifically Nakamura.

In a similar field of endeavor Nakamura discloses a solid state image sensing device. Nakamura discloses a timing diagram figure 10. This diagram discloses a signal, Read1 (19-1 figure 10) which is the signal sent to the gate electrode of the transfer transistor. The diagram discloses a second signal, Reset1 (20-1 figure 10) which is the signal sent to the gate electrode of the reset transistor. These signals are equivalent to V21 (figure 6f) and V24 (figure 6e) of the application, respectively. Figures 6 (e &f) teach that the samplings and holdings of precharge phase and data phase are the time periods after a reset pulse and before a transfer pulse; and after a transfer pulse and before a second reset pulse. Figure 10 teaches that during these periods the reset pulse, Reset1, is at the ground potential.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the timing diagram taught by Nakamura, specifically wherein at both timings of sampling and holding a precharge phase and a data phase, the gate potential of the reset transistor is set at the ground potential, in the solid-state

imaging device taught by Nakamura and Hashimoto, for the purpose of stabilizing the device.

Regarding claim 8, a camera system having: an optical system for guiding incident light to an imaging portion of the solid state imaging device; and a signal processing circuit for processing an output signal of the solid state imaging device, a solid state imaging device with a unit pixel having a photoelectric converter for generating a charge in accordance with an amount of incident light, and a reset transistor for resetting the floating node, at least one of a plurality of potentials supplied to a gate electrode of the reset transistor being a negative potential, however, Hashimoto fails to disclose a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line (both transistors are part of the unit pixel of the solid state imaging device). However, the examiner maintains that it was well known in the art to disclose a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line (both transistors are part of the unit pixel of the solid state imaging device), as taught by Nakamura.

In a similar field of endeavor Nakamura discloses a solid state imaging device. Specifically Nakamura discloses a solid state imaging device with a unit pixel having a transfer transistor for transferring a signal of the photoelectric converter to a floating node (2-1 figure 9), an amplifier transistor for outputting a signal of the floating node to a signal line (3-1 figure 9), as disclosed at paragraph 15, lines 2-5.

Therefore it would have been obvious to one or ordinary skill in the art at the time the invention was made to modify Hashimoto by specifically providing a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line (both transistors are part of the unit pixel of the solid state imaging device), as taught by Nakamura, for the purpose of providing a camera with a more stable solid state imaging device.

Regarding claim 9, Hashimoto discloses a camera system having: an optical system for guiding incident light to an imaging portion of the solid state imaging device; and a signal processing circuit for processing an output signal of the solid state imaging device, a solid state imaging device with a unit pixel having a photoelectric converter for generating a charge in accordance with an amount of incident light, and a reset transistor for resetting the floating node, and a portion able to supply three or more types of potentials to the gate electrode of the reset transistor, however, Hashimoto fails to disclose a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line (both transistors are part of the unit pixel of the solid state imaging device). However, the examiner maintains that it was well known in the art to provide a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line (both transistors as part of a unit pixel of a solid state imaging device), as taught by Nakamura.

In a similar field of endeavor Nakamura discloses a solid state imaging device. Specifically Nakamura discloses a solid state imaging device with a unit pixel having a transfer transistor for transferring a signal of the photoelectric converter to a floating node (2-1 figure 9), an amplifier transistor for outputting a signal of the floating node to a signal line (3-1 figure 9), as disclosed at paragraph 15, lines 2-5.

Therefore it would have been obvious to one or ordinary skill in the art at the time the invention was made to modify Hashimoto by specifically providing a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line (both transistors are part of the unit pixel of the solid state imaging device), as taught by Nakamura, for the purpose of providing a camera with a more stable solid state imaging device.

Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Hashimoto and further in view of Mabuchi (Japanese patent application publication 2000-092392), hereinafter referenced as Mabuchi.

Regarding claim 6, Nakamura and Hashimoto disclose everything claimed as applied above (see claim 5), however the pair fail to disclose wherein during a period which the gate potential of the reset transistor of the selected pixel is set at the ground potential, the gate potential of the reset transistor of the nonselected pixel is a negative potential. However, the examiner maintains that it was well known in the art to provide wherein during a period which the gate potential of the reset transistor of the selected

pixel is set at the ground potential, the gate potential of the reset transistor of the nonselected pixel is a negative potential, as taught by Mabuchi.

In a similar field of endeavor Mabuchi discloses a solid-state image pickup device. In addition Mabuchi discloses the potential of the reset control line 12 (figure 1) of a non-choosing line, i.e., the gate potential of the reset transistor 3, serves as a negative value, as taught in paragraph 21 lines 4-6 of the attached translation. Mabuchi teaches that the negative potential which is supplied is created by turning on a control transistor (14 figure 1) of a non-choosing line. Since the control transistor (14 figure 1) of the choosing line is turned off, a negative potential cannot be supplied to the choosing line. Normal operation of the pixel requires the gate electrode of the reset transistor to be both on (positive potential supplied to the gate electrode) and off (ground potential supplied to the gate electrode). From this is can derived that in a period during which the gate potential of the reset transistor of the selected pixel is set at the ground potential, the gate potential of the reset transistor of the nonselected pixel is a negative potential.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura and Hashimoto by specifically providing wherein during a period which the gate potential of the reset transistor of the selected pixel is set at the ground potential, the gate potential of the reset transistor of the nonselected pixel is a negative potential, as taught by Mabuchi, for the purpose of reducing power supply voltage.

Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Nakamura et al. (United States patent 6,873,034), hereinafter referenced as '034.

Regarding claim 7, Nakamura discloses everything as claimed above (see claim 1), however, Nakamura fails to disclose wherein the device has a chip for processing the signal output through the signal line. However, the examiner maintains that it was well known in the art to provide wherein the device has a chip for processing the signal output through the signal line, as taught by '034.

In a similar field of endeavor '034 discloses a solid-state imaging device. In addition '034 discloses a chip (30 figure 1) having an integrated circuit (7 figure 1) for processing an image signal output from an output terminal of the solid-state imaging element, as disclosed at column 5, lines 58-63.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura by specifically providing wherein the device has a chip for processing the signal output through the signal line, as taught by '034, for the purpose of allowing for possible storage of the image.

Conclusion

.Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON FLOHRE whose telephone number is (571)270-7238. The examiner can normally be reached on Monday to Thursday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffery Harold can be reached on 571-272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jefferey F Harold/
Supervisory Patent Examiner, Art Unit 4112